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Chips, dies, chiplets and dielets and heterogeneous integration (of course!)

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Abstract

Packaging is undergoing a major paradigm shift and promises to take up the lag caused by the slowing down of CMOS scaling. In this paper, we examine these shifts that have been driven by the scaling of key packaging metrics such as bump pitch, trace pitch, inter-die spacing and alignment. The goal of advanced packaging is to enable the same benefits that Moore/Dennard scaling has accomplished for CMOS viz. density, performance, power, and cost. The vehicles that advanced packaging employs are somewhat different: dielets/chiplets, advanced assembly techniques, simplified inter-chip communication protocols and cost optimization via the use of optimized heterogeneous technologies. Another important aspect of advanced packaging is the adoption and adaptation of silicon technology methods to packaging.
In this talk we will discuss the technologies and some instantiation examples that we have developed at UCLA.
(Keywords: Packaging, chiplets, dielets, Si IF, FOWLP, interposers, 3DIC)