Technology Inflection Points in Logic Semiconductor Technology: What next?

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Since 2010, the usage of mobile products such as smartphones, tablets, wearables, etc. has increased significantly, and now it is difficult to imagine everyday life without mobile products. In these environmental changes, consumers want to buy a cheaper mobile product with faster speed, various functions and longer battery life. To achieve market requirements, low power devices are essential and must meet all aspects of logic technology criterions: Power, Performance, and Area. In logic applications, traditional planar Si-MOSFETs had been successfully expanded for decades according to Moore's law by adopting technical innovations such as stress engineering, high-k metal gate and gate last scheme. As the gate length continuously decreases further, however, the source-to-drain leakage has been no longer controlled by gate with a planar structure due to the severe short channel effects (SCEs). For breakthroughs of scaling limit, then, structure innovations have been introduced because of not only superior electrostatic control of the channel potential but also novel CMOS process compatibility.

Since FinFET has replaced planar FET as a mainstream high-technology, FinFET has overcome the technical limitations through continuous development for the past decade. The tapered Fin structure has been changed to the vertical fin structure with narrower Fin width to further improve SCEs and enables gate length scaling. The increase in resistance due to the contact poly pitch (CPP) scaling has been solved by increasing Fin height and improving source-drain (SD) stress engineering technology. In addition, despite the slowdown of CPP scaling, various hyper scaling technologies such as singe diffusion break (SDB) and gate contact on active have enabled the area scaling, satisfying the area reduction required in the market. Because continuous improvement of intrinsic transistor and device scaling made improvement of parasitic component more important, low resistance conductors and lower-k dielectric materials have been introduced in middle of line and back end of line in recent years for the further extension of technologies.

In spite of the long technical evolution, FinFET CMOS scaling in below 3nm nodes, have no choice but to face a plateau of performance improvement, fundamental subthreshold leakage issues and reliability problems between gate and contact. Various candidates, including tunnel-FET (TFET), negative capacitance FET (NCFET), and III-V FETs to replace FinFET technologies, have been studied in depth for a long time in academia, research institutes and major companies. However, most of them have been eliminated from the competition, due to the fundamental problems such as lower current drivability, no reliable control for multi-Vth, and hysterisis issue. Multi bridge channel FET (MBCFET^{TM}), meanwhile, has been considered the most likely to replace the former FinFET technology with excellent gate control, increased effective channel width, and process compatibility. [1-4] Structural innovations from FinFET to GAA MBCFET^{TM} are now occurring by solving various critical problems such as defective SD EPI growth and multiple Vt processes and inhibiting lower substrate leakage. Samsung has already started producing 3 nm chips using MBCFET^{TM} technology in 2022, and TSMC announced a timetable for commercializing the 2nm GAA process in 2025.

Although the GAA MBCFET^{TM} conversion has given the technology inflection point of transistor, Si -based transistor technology is expected to show limitations in terms of CPP and standard cell height scaling after technical evolution of GAA MBCFET^{TM} in a decade. Continuous area scaling and chip level performance improvement are expected to be achieved by the introduction of innovative 3D integration technology and material innovations. [5] Layout efficiency will be improved with vertically stacked PFET on NFET or vice versa, which will continue to improve area scaling and performance. Besides, introduction of innovative materials such as 2D transition metal di-chalcogenide (TMD) channel and low resistance bi-metal will enable further gate length and metal pitch scaling, respectively.

The technical limitations have been faced with FinFET's long developments, however, the explosive growth of data and connectivity still requires continuous development of the semiconductor technology. Currently, the introduction of GAA MBCFET^{TM} is a technical inflection point, which is solving the problem of scaling and performance, and the future will be prepared through the study of 3D stacked FET and innovative material.

[1] S.-Y. Lee et al. Symposium on VLSI 2004 [2] E. Yoon et al. IEDM 2004. [3] M. S. Kim et al. Symposium on VLSI 2006. [4] G. Bae et al. IEDM 2018. [5] C.-Y. Huang et al. IEDM 2020.